Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **S**
2. **1I0**
3. **1I1**
4. **1Y**
5. **2I0**
6. **2I1**
7. **2Y**
8. **GND**
9. **3Y**
10. **3I1**
11. **3I0**
12. **4Y**
13. **4I1**
14. **4I0**
15. **N.E**
16. **VCC**

**.048”**

**.068”**

**8 9**

**2 1 16 15**

**3**

**4**

**5**

**6**

**7**

**14**

**13**

**12**

**11**

**10**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: FLOAT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .048” X .068” DATE: 3/14/19**

**MFG: ZYTREX THICKNESS .000” P/N: 54LS157**

**DG 10.1.2**

#### Rev B, 7/1